I CLAIM:

1. A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction, a surface depletion region of the body region extending along the dielectric layer below the gate electrode and being spaced apart from a body contact portion of the body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region; and

electronic circuitry having a capacitance signal path for receiving the varactor to enable the circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

2. A structure as in Claim 1 wherein the circuitry comprises at least one additional region of the semiconductor body.

3. A structure as in Claim 1 wherein the circuitry comprises an inductor.

4. A structure as in Claim 1 wherein the plate electrode is at a plate-to-body bias voltage relative to the body electrode, the gate electrode is at a gate-to-body bias voltage relative to the body electrode, and the gate-to-body voltage is maintained approximately constant as the plate-to-body voltage is varied.

5. A structure as in Claim 1 wherein the plate electrode is at a plate-to-body bias voltage relative to the body electrode, the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differs from the plate-to-body voltage, and the gate-to-body voltage is varied as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

6. A structure as in Claim 5 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

7. A structure as in Claim 5 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

8. A structure as in Claim 1 wherein the plate and body regions extend to a primary surface of the semiconductor body.

9. A structure as in Claim 7 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurs in the body region under control of the plate and gate electrodes, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

10. A structure as in Claim 8 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

11. A structure as in Claim 8 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

12. A structure comprising:

a varactor comprising (a) a plate region and body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction, a surface depletion region of the body region extending along the dielectric layer below the gate electrode and being spaced apart from a body contact portion of the

body region, the body contact portion contacting the body electrode and being more heavily doped than the surface depletion region; and

electronic circuitry comprising an inductor situated in an inductance-capacitance signal path with the plate and body electrodes to form an oscillatory inductive-capacitive combination.

13. A structure as in Claim 12 wherein the plate electrode is at a plate-to-body bias voltage relative to the body electrode, the gate electrode is at a gate-to-body bias voltage relative to the body electrode, and the gate-to-body voltage is maintained approximately constant as the plate-to-body voltage is varied.

14. A structure as in Claim 12 wherein the plate electrode is at a plate-to-body bias voltage relative to the body electrode, the gate electrode is at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differs from the plate-to-body voltage, and the gate-to-body voltage is varied as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

15. A structure as in Claim 14 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

16. A structure as in Claim 14 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

17. A structure comprising:

a plate region and body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;

a dielectric layer situated over the semiconductor body and contacting the body region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage being maintained approximately constant as the plate-to-body voltage is varied.

18. A structure as in Claim 17 further including componentry for maintaining the gate-to-body voltage approximately constant.

19. A structure as in Claim 17 wherein the plate and body regions extend to a primary surface of the semiconductor body.

20. A structure as in Claim 19 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurs in the body region under control of the plate and gate electrodes, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

21. A structure as in Claim 19 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

22. A structure as in Claim 21 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

23. A structure comprising:

a plate region and body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction;

a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode;

a dielectric layer situated over the semiconductor body and contacting the body region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the gate-to-body voltage differing from the plate-to-body voltage, the gate-to-body voltage varying as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

24. A structure as in Claim 23 wherein the gate-to-body voltage varies approximately linearly with the plate-to-body voltage.

25. A structure as in Claim 23 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.

26. A structure as in Claim 23 further including componentry for causing the gate-to-body voltage to vary as a function of the plate-to-body voltage.

27. A structure as in Claim 26 wherein the componentry causes the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

28. A structure as in Claim 23 wherein the plate and body regions extend to a primary surface of the semiconductor body.

29. A structure as in Claim 23 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurs in the body region under control of the plate and gate electrodes, the inversion layer occupies a lateral inversion area along the primary surface, and the varactor has a maximum capacitance dependent on the inversion area in combination with the plate area.

30. A structure as in Claim 28 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region.

31. A structure as in Claim 29 wherein the plate region comprises a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

32. A structure comprising:

a plate region and a body region of a semiconductor body, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions extending to a primary surface of the semiconductor body and meeting each other to form a p-n junction, the plate region comprising a main plate portion and at least one finger portion continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong;

a dielectric layer situated over the semiconductor body and contacting the plate region; and

a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region.

33. A structure as in Claim 32 wherein each finger is of lesser average dimension perpendicular to that finger than is the main plate portion.

34. A structure as in Claim 32 wherein the body region substantially laterally surrounds, and extends below substantially all of, the plate region including each finger.

35. A structure as in Claim 32 further including a field insulating region extending into the semiconductor body along its primary surface, the field insulating region laterally adjoining the body region.

36. A structure as in Claim 32 wherein there are at least two finger portions.

37. A structure as in Claim 32 wherein there are at least four finger portions.

38. A method comprising:

selecting a varactor which comprises (a) a plate region and a body region of a semiconductor body, (b) a dielectric layer situated over the semiconductor body and

contacting the body region, and (c) a gate electrode situated over the dielectric layer at least where the dielectric layer contacts material of the body region, the body region being of a first conductivity type, the plate region being of a second conductivity type opposite to the first conductivity type, the plate and body regions meeting each other to form a p-n junction and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region occurring in the body region under control of the plate and gate electrodes, the inversion layer occupying a lateral inversion area along the primary surface, the varactor having a maximum capacitance dependent on the inversion area in combination with the plate area; and

adjusting the plate and inversion areas to control the minimum and maximum capacitances of the varactor.

39. A method as in Claim 38 wherein the minimum capacitance is approximately proportional to the plate area, and the maximum capacitance is approximately proportional to an accumulative combination of the inversion and plate areas.

40. A method as in Claim 38 wherein the adjusting step involves adjusting the ratio of the inversion area to the plate area in order to achieve at least a specified value of the ratio of the maximum capacitance to the minimum capacitance.

41. A method as in Claim 38 wherein the selecting act includes configuring the body to substantially laterally surround, and extend below substantially all of, the plate region.

42. A method as in Claim 38 wherein the selecting and adjusting acts include configuring the plate region to comprise a main plate portion and at least one finger continuous with the main plate portion, extending laterally away from the main plate portion, and meeting the body region therealong.

43. A method as in Claim 38 wherein the selecting act includes providing the varactor with a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body

electrode, the gate electrode being at a gate-to-body bias voltage relative to the body electrode, the method further including maintaining the gate-to-body voltage approximately constant as the plate-to-body voltage is varied.

44. A method as in Claim 38 wherein the selecting act includes providing the varactor with a plate electrode and a body electrode respectively connected to the plate and body regions, the plate electrode being at a plate-to-body bias voltage relative to the body electrode, the gate electrode being at gate-to-body bias voltage relative to the body electrode, the method further including causing the gate-to-body voltage to differ from the plate-to-body voltage and to vary as a function of the plate-to-body voltage as the plate-to-body voltage is varied.

45. A method as in Claim 44 wherein the causing act entails causing the gate-to-body voltage to vary approximately linearly with the plate-to-body voltage.

46. A method as in Claim 44 wherein the gate-to-body voltage differs by approximately a constant non-zero amount from the plate-to-body voltage.